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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,755	04/09/2004	Masanao Yokoyama	8019-1039	8776

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EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/820,755	YOKOYAMA, MASANAO	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8,9,11,13-20* is/are rejected.

7)☒ Claim(s) *6,7,10 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/9/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/820,755 filed 04/09/2004.

2. Claims 1-20 are pending in the Application.

Drawings

3. The drawings are objected to because Figures 7 and 8 have contradictory labels. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

There is a contradiction between Figures and their description in the Specification, such as Figures 7 and 8 have a label 100 as a header, while description

(for example Page 5) refers the number **100** to the repeater and hard macro at the same time. It is not clear where in the Figures repeater 100 is depicted.

Specification

4. The abstract of the disclosure is objected to because

- description on the pages 5, 6, 7 does not refer to the Figure(s) number while identifying elements from the Figures.
- Abstract line 8 after "starts" insert –at--
- Specification, for example, Pages: 2 (last paragraph), 5 (second paragraph), 6 (third paragraph), 7 (first line) have error as missing –at—before "a first outer edge".

Correction is required. See MPEP § 608.01(b).

Claim Objections

5. Claims 1, 15, 17 and 19 are objected to because of the following informalities:

Claim 1 line 4 after "starts" insert –at--

Claim 15 line 5 after "starts" insert –at--

Claim 17 line 6 after "starts" insert –at--

Claim 19 line 6 after "starts" insert –at--

Appropriate correction is required.

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. Claims 19 and 20 are rejected under 35 U.S.C. 101 because

the claimed invention is directed to non-statutory subject matter. A program for causing a computer to analyze a floor-plan is descriptive material and is nor statutory if not claimed as embodied (executed) in computer-readable media, because without executing, the program is not capable of causing functional change in the computer.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 19 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claims 17 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: analysis of a floor-plan of a semiconductor integrated circuit, since "a device for analyzing a floor-plan of a semiconductor integrated circuit" is claimed in a preamble of the claim 17 without any further steps showing the analysis of the floor-plan of IC in the limitations; instead, the limitations of the claim 17 point out arranging a hard macro on the semiconductor chip. Furthermore, claim 18, which depends on claim 17, claims a vague step of analyzing a route of the wire without giving any specifics of an analysis and its results. For the examination purposes Examiner will consider only part of the claims 17 and 18 containing the structure of the hard-macro, since it is a gap between analyzing a floorplan of IC including a hard-macro and describing the structure of the hard-macro.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Takahashi (US Patent 5,331,572).

With respect to claim 1-5, 8, 9 and 11 Takahashi teaches a hard-macro arranged on a semiconductor chip for constituting a part of a semiconductor integrated circuit as shown on the Fig. 17 input/output block 37 arranged in the corner of the semiconductor chip (col. 1, ll.36-37), including at least one wire passing therethrough, wherein the wire is formed in the hard-macro before the hard-macro is arranged on the semiconductor chip within power supply wiring patterns 41 included in the input-output block 37 as shown on the Fig. 19 (43-45), and the wire starts at a first outer edge of the hard-macro and terminates at a second outer edge of the hard-macro intersecting with the first outer edge as shown on the Fig. 19 the wiring pattern 41 passing through input-output block 37 starting at one outer edge of the block 37 (input) and ending in the other outer edge of the block 37 (output) (col. 1, ll.46-47).

With respect to claims 2-5, 8, 9 and 11 Takahashi teaches:

Claims 2: wherein the first and second outer edges are adjacent to each other as shown on the Fig. 19 the wiring pattern arranged on the block 37 such as input on one outer edge and the output on the adjacent outer edge;

Claim 4: wherein the wire is L-shaped as shown on the Fig. 19 wiring pattern 41 is arranged on the block 37 in L-shape;

Claim 5: wherein the wire is linear as shown on the Fig. 19 wiring pattern 41 is arranged on the block 37 by linear wires;

Claim 8: further including a repeater inserted in the wire within inserting buffer including wiring pattern 40 as shown on the Fig. 18, wherein wiring pattern 40 connected to the wiring pattern 41 (col. 1, ll.42-44);

Claim 9: wherein the hard-macro includes a plurality of wires passing therethrough within wiring pattern 41 as shown on the Fig. 19 passing through input/output/ block 37, wherein wiring pattern includes plurality of wires;

Claim 11: wherein at least one of the wires includes a repeater inserted therein wire within inserting buffer including wiring pattern 40 as shown on the Fig. 18, wherein wiring pattern 40 connected to the wiring pattern 41 (col. 1, ll.42-44).

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

14. Claims 1-5, 8, 9, 11, 13, 15-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Sasaki (US Patent 6,529,039)

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

With respect to claim 1 Sasaki teaches a hard-macro arranged on a semiconductor chip for constituting a part of a semiconductor integrated circuit within macro cell 3 shown on the fig. 8, wherein macro cell 3 arranged on the chip 30, including at least one wire passing therethrough within wiring passing through macro cell 3 as shown on the Fig. 8, wherein the wire is formed in the hard-macro before the hard-macro is arranged on the semiconductor chip within configuration of macro cell 3 shown on the Fig. 7 for further arrangement macro cell 3 on the chip 30 as shown on the Fig. 8 (col. 5, ll.26-30; col. 3, ll.58-63), and the wire starts at a first outer edge of the hard-macro as shown on the Fig. 8 the wire starts at a first outer upper side of the macro cell 3 at terminal "c" and terminates at a second outer edge of the hard-macro intersecting with the first outer edge within traversing the wire and ending at a second right side of the macro cell 3 at terminal "f" (col. 10, ll.51-53, ll.57-59).

With respect to claim 15 Sasaki teaches a semiconductor integrated circuit including a hard-macro arranged on a semiconductor chip for constituting a part of the semiconductor integrated circuit (col. 1, ll. 6-9), including at least one wire passing therethrough within wiring passing through macro cell 3 as shown on the Fig. 8, wherein

the wire is formed in the hard-macro before the hard-macro is arranged on the semiconductor chip within configuration of macro cell 3 shown on the Fig. 7 for further arrangement macro cell 3 on the chip 30 as shown on the Fig. 8 (col. 5, ll.26-30; col. 3, ll.58-63), and the wire starts at a first outer edge of the hard-macro as shown on the Fig. 8 the wire starts at a first outer upper side of the macro cell 3 at terminal "c" and terminates at a second outer edge of the hard-macro intersecting with the first outer edge within traversing the wire and ending at a second right side of the macro cell 3 at terminal "f" (col. 10, ll.51-53, ll.57-59).

With respect to claim 17 Sasaki teaches a semiconductor integrated circuit including a hard-macro arranged on a semiconductor chip for constituting a part of the semiconductor integrated circuit (col. 1, ll. 6-9), including at least one wire passing therethrough within wiring passing through macro cell 3 as shown on the Fig. 8, wherein the wire is formed in the hard-macro before the hard-macro is arranged on the semiconductor chip within configuration of macro cell 3 shown on the Fig. 7 for further arrangement macro cell 3 on the chip 30 as shown on the Fig. 8 (col. 5, ll.26-30; col. 3, ll.58-63), and the wire starts at a first outer edge of the hard-macro as shown on the Fig. 8 the wire starts at a first outer upper side of the macro cell 3 at terminal "c" and terminates at a second outer edge of the hard-macro intersecting with the first outer edge within traversing the wire and ending at a second right side of the macro cell 3 at terminal "f" (col. 10, ll.51-53, ll.57-59).

With respect to claims 2-5, 8, 9, 11, 13, 16 and 18 Sasaki teaches:

Claim 2: wherein the first and second outer edges are perpendicular to each other as shown on the Fig. 8 the upper side of the macro cell 3 (where the wire starts) is perpendicular to the right side of the macro cell 3 (where the wire terminates);

Claim 3: wherein the first and second outer edges are adjacent to each other as shown on the Fig. 8 the upper side of the macro cell 3 (where the wire starts) is adjacent to the right side of the macro cell 3 (where the wire terminates);

Claim 4: wherein the wire is L-shaped as shown on the Fig. 8 the wire traversing from the upper side of the macro cell 3 to the right side of the macro cell 3 has L-shape;

Claim 5: wherein the wire is linear as shown on the Fig. 8 the wire traversing from the upper side of the macro cell 3 to the right side of the macro cell 3 is linear;

Claim 8: further including a repeater inserted in the wire within inserting a buffer 28 in the wire as shown on the Fig. 7, wherein the configuration of the macro cell 3 is depicted and arranged in the chip (fig. 8) (col. 9, ll.63-64);

Claim 9: wherein the hard-macro includes a plurality of wires passing therethrough as shown on the Fig. 8 the macro cell 3 includes plurality of wires passing through macro cell 3 ;

Claim 11: wherein at least one of the wires includes a repeater inserted therein within inserted buffer 28 in the wire as shown on the Fig. 7, wherein the configuration of the macro cell 3 is depicted and arranged in the chip (fig. 8) (col. 9, ll.63-64);

Claim 13: wherein the hard-macro is a random access memory (RAM) (col. 1, ll.17-18);

Claim 16: wherein the semiconductor integrated circuit is a cell base integrated circuit (CBIC) within arranging macro cells on a chip and connecting them to realize a system LSI having various functions dedicated to a particular user (col. 1, ll.16-21);

Claim 18 wherein the device analyzes a route of the wire within analyzing the wire route and selecting an optimal wire route, which is typically performed by routing tool during the design of the semiconductor integrated circuit (col. 15, ll.62-64).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 1 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bednar et al. (US Patent 6,543,040) in view of Kaneko (US Patent Application Publication 20010025364).

With respect to claim 1 Bednar teaches a hard-macro arranged on a semiconductor chip for constituting a part of a semiconductor integrated circuit a method for preparing the macros for anticipated stage wiring for arranging on the integrated circuit (col. 1, ll.53-54; ll.57-61), including at least one wire passing therethrough, wherein the wire is formed in the hard-macro before the hard-macro is arranged on the semiconductor chip within pre-designed macro 112 as shown on the Fig. 2 accommodating wiring 118 and 120, which are passing through the macro 112 (col. 3, ll.38-41), and the wire starts at a first outer edge of the hard-macro and

terminates at a second outer edge of the hard-macro intersecting with the first outer edge as shown on the Fig. 2, for example wire 118 starts at a first outer edge of the macro 112 and terminates at a second outer edge of the macro 112 by passing through the macro 112 (col. 3, ll.41-48).

With respect to claim 14 Bednar teaches the limitations from which the clam depends. However Bednar lacks the specifics regarding a type of macros arranged on the semiconductor chip. Kaneko teaches the hard-macro is a phase-locked loop (PLL) as shown on the Fig. 2 depicting typical arrangement macro cells on the semiconductor chip 200, wherein one of the plurality of macro cells is PLL 205 (paragraph [0006]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used Kaneko to teach the specifics subject matter Bednar does not teach, because the standard cell (chip) constructed by interconnecting plurality of macros, wherein one of the macros is PLL (abstract; paragraph [0038]).

Allowable Subject Matter

17. Claims 6, 7, 10 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach arranging the wires passing through a hard macro, when hard macro has a cutout including one of the corners of the hard macro, and the wire extends along the cutout between the first and second outer edges; wherein the plurality of wires passing through the hard macro are arranged with an equal distance between them; wherein the wire is divided into a plurality of portions each of which is arranged in each of a plurality of

hierarchies of the hard macro, wherein the plurality of wires passing thorough the hard macro as claimed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

JACK CHIANG
SUPERVISORY PATENT EXAMINER